What is Claimed is:

1. Circuitry for providing a dynamically adjustable bandwidth comprising:

a phase frequency detector receiving as input a clock signal and having a signal output;

a charge pump having a pump input coupled to the signal output of the phase frequency detector and having a pump output;

a loop filter having a filter input coupled to the pump output of the charge pump and having a filter output;

a voltage controlled oscillator having an oscillator input coupled to the filter output of the loop filter and having an oscillator output;

a divider circuit having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector; and

control circuitry that receives as input at least one control signal and is operative to dynamically adjust a setting in at least one of the charge pump, the loop filter, the voltage controlled oscillator, and the divider circuit while the circuitry is processing data.

2. The circuitry of claim 1 wherein the circuitry is clock data recovery circuitry.

3. The circuitry of claim 1 wherein the circuitry is phase locked loop circuitry.

4. The circuitry of claim 1 wherein the setting in the charge pump that can be dynamically adjusted is current.

5. The circuitry of claim 1 wherein the setting in the loop filter that can be dynamically adjusted is at least one of a resistor value and a capacitor value.

6. The circuitry of claim 1 wherein the setting in the voltage controlled oscillator that can be dynamically adjusted is a voltage gain.

7. The circuitry of claim 1 wherein the setting in the divider circuit that can be dynamically adjusted is a scale factor.

8. The circuitry of claim 1 wherein the at least one control signal includes a value for the setting.

9. The circuitry of claim 1 wherein the at least one control signal is indicative of whether a value of the setting is to be increased or decreased.

10. The circuitry of claim 1 wherein the at least one control signal includes at least one data bit that corresponds to information on a value for the setting stored in a lookup table in the control circuitry.

11. The circuitry of claim 1 wherein the at least one control signal is set by a programmable logic device.

12. The circuitry of claim 1 wherein the at least one control signal is set by circuitry external to a programmable logic device.

13. The circuitry of claim 1 wherein the at least one control signal is set by user input.

14. A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

circuitry as defined in claim 1 coupled to the processing circuitry and the memory.

15. A printed circuit board on which is mounted the apparatus as defined in claim 1.

16. The printed circuit board defined in claim 15 further comprising:

a memory mounted on the printed circuit board and coupled to the circuitry.

17. The printed circuit board defined in claim 15 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the apparatus.

18. A programmable l ogic device comprising:

clock data recovery (CDR) circuitry that receives as input a reference clock signal and a CDR signal and is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal, and to use the recovered clock signal to recover clock information and data information from the

CDR signal; and

control circuitry that receives as input at least one control signal and is operative to dynamically adjust a bandwidth of the CDR circuitry by changing a setting in at least one component in the CDR circuitry while the CDR circuitry is processing data.

19. The programmable logic device of claim 18 wherein the CDR circuitry comprises:

a phase frequency detector receiving as input the reference clock signal and having a signal output;

a charge pump having a pump input coupled to the signal output of the phase frequency detector and having a pump output;

a loop filter having a filter input coupled to the pump output of the charge pump and having a filter output;

a voltage controlled oscillator having an oscillator input coupled to the filter output of the loop filter and having an oscillator output; and

a divider circuit having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector.

20. The programmable logic device of claim 19 wherein the at least one component comprises one of the charge pump, the loop filter, the voltage controlled oscillator, and the divider circuit.

21. The programmable logic device of claim 19 wherein the setting in the at least one component comprises current in the charge pump.

22. The programmable logic device of claim 19 wherein the setting in the at least one component comprises a resistor value in the loop filter.

23. The programmable logic device of claim 19 wherein the setting in the at least one component comprises a capacitor value in the loop filter.

24. The programmable logic device of claim 19 wherein the setting in the at least one component comprises a voltage gain in the voltage controlled oscillator.

25. The programmable logic device of claim 19 wherein the setting in the at least one component comprises a scale factor in the divider circuit.

26. The programmable logic device of claim 18 wherein the at least one control signal is set by the programmable logic device.

27. The programmable logic device of claim 18 wherein the at least one control signal is set by circuitry external to the programmable logic device.

28. The programmable logic device of claim 18 wherein the at least one control signal is set by user input.

29. A programmable logic device comprising:

phase locked loop (PLL) circuitry that receives as input a clock signal and is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the clock signal; and

control circuitry that receives as input at least one control signal and is operative to dynamically adjust a bandwidth of the PLL circuitry by changing a setting in at least one component in the PLL circuitry while the PLL circuitry is processing data.

30. The programmable logic device of claim 29 wherein the PLL circuitry comprises:

a phase frequency detector receiving as input the reference clock signal and having a signal output;

a charge pump having a pump input coupled to the signal output of the phase frequency detector and having a pump output;

a loop filter having a filter input coupled to the pump output of the charge pump and having a filter output;

a voltage controlled oscillator having an oscillator input coupled to the filter output of the loop filter and having an oscillator output; and

a divider circuit having a divider input coupled to the oscillator output of the voltage controlled oscillator and having a divider output that feeds back to the input of the phase frequency detector.

31. The programmable logic device of claim 30 wherein the at least one component comprises one of the charge pump, the loop filter, the voltage controlled oscillator, and the divider circuit.

32. The programmable logic device of claim 30 wherein the setting in the at least one component comprises current in the charge pump.

33. The programmable logic device of claim 30 wherein the setting in the at least one component comprises a resistor value in the loop filter.

34. The programmable logic device of claim 30 wherein the setting in the at least one component comprises a capacitor value in the loop filter.

35. The programmable logic device of claim 30 wherein the setting in the at least one component comprises a voltage gain in the voltage controlled oscillator.

36. The programmable logic device of claim 30 wherein the setting in the at least one component comprises a scale factor in the divider circuit.

37. The programmable logic device of claim 29 wherein the at least one control signal is set by the programmable logic device.

38. The programmable logic device of claim 29 wherein the at least one control signal is set by circuitry external to the programmable logic device.

39. The programmable logic device of claim 29 wherein the at least one control signal is set by user input.